

ML4039E

Technical Reference and user manual

400G Bit Error Ratio Tester



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1. General Description

The ML4039E is a fully featured 400G BERT that can be configured as a 4x53.125 GBaud BERT. At high rates (53 Gbaud) and low rates (25 Gbaud) both NRZ and PAM4 modes are supported. It is used in Production testing of transceivers as for Functional and SI testing.

The ML4039E is designed for 400G applications. This instrument is a fully integrated, ultracompact, USB/Fast Ethernet controlled instrument that combines all the functions and features of a signal generator, bit error-ratio tester and data analysis system with Post-Emphasis and Pre-Emphasis, 7 taps FIR capabilities.

2. Ordering information

The instrument can be ordered with the following part number.

ML4039E	4 channels BERT
ML4039EN	4 channels BERT with Noise injection feature

Table 1: Hardware ordering information

For more details please refer to the below link: For ML4039E: <u>https://multilaneinc.com/product/ML4039e/</u> For ML4039EN: <u>https://multilaneinc.com/product/ml4039en/</u>

3. Operating conditions

A 110/220V adapter is used to power-up the board.

If the temperature of the board inside the box has surpassed the 70°C value, in order to prevent overheating, this temperature is considered as the cutoff value.

The instrument will resume normal functionality again once the temperature is within the optimal range.

4. Block Diagram

The ML4039E block diagram is illustrated in figure 1. Signals are transmitted from the TX side through four independent channels, and the received signals are routed from the RX side of the error detector. These signals can be monitored and controlled channel by channel.





Figure 1: Block Diagram of the ML4039E

5. Hardware design overview

Figure 2 shows a general view of the ML4039E.



Figure 2: ML4039E mechanical drawing



The instrument dimensions in mm are shown in figures 3 and 4.

With an overall weight of two kilograms.

The back plate includes an ON-OFF switch button, Ethernet and USB ports. A 110/220V power adapter can be connected to supply the board with the required power.

The faceplate shows an SMA connector for clock out.

Also the faceplate shows sixteen connectors type K (2.92mm connectors) that are used to connect to the four differential TX and RX channels. Once powered up, and the switch button turned on, the board should be able to perform all the required measurements.

6. Clock Configuration

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The ML4039E supports output clock. The user can switch between two options the reference clock and monitor clock. The monitor clock supports the following rate dividers: 4, 8, 16, 32, 64, and 128. Rate divider 4 is currently only supported at low rates.

The reference clock has an optimal value of 156.25 MHz.

In the current hardware revision, external clock option is not supported.

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7. Transmitter side characteristics

As described above the TX signals are transmitted through four independent channels.

The Low voltage settings or high voltage settings for each channel, generated during the calibration process, at scaling 80% (for low voltage) or 100% (for high voltage), is being applied at high and low rates, and in both eye modes: NRZ and PAM4.

These settings once applied and saved, during calibration, ensure that the ML4039E performs all the required measurements in optimal mode.

These settings can be controlled by the user in advanced mode, in this way the user can control all the TX settings including: TX pattern, amplitude, Pre-emphasis, Main Tap, Post-Emphasis or the 7 FIR taps...

The ML4039E operates in PAM4 and NRZ modes, on numerous bitrates.

The BERT locks on all the supported rates, amplitudes and patterns. The parameters are mentioned in table 2.

The TX Equalization is a digital combination of FFE and DFE. PAM4 gray coding is also supported. Test pattern generator per lane includes error injection.

The patterns, error insertion and emphasis taps can be checked and controlled per lane. The user could turn off and disable the TX side channel by channel.

Kindly refer to the user manual paragraph 11 for more details on how to operate the ML4039E.

Table 2 shows the TX Output Characteristics of the ML4039E.



	Parar	neter		Typical	Maximum	Unit	
Line Date	NRZ	IRZ		22.75 – 29.25 45.5 – 56	up to 29.25 (low rate) up to 56 (high rate)	Gbps	
Line Kate	PAM4			22.75 – 29.25 45.5 – 55.5	up to 29.25 (low rate) up to 55.5 (high rate)	Gbaud	
Clock-out Amplitude	9			ТВ	D	mV	
Clock-out	Monitor			Rate dividers: 4, 8, 16, 32, 64, 128	Up to Rate/4 (at low rates)	MHz	
Frequency	equency Reference			156.25	133.82 -165		
	Reference 156.25 133.82 - 165 Low Rate (NRZ& Advanced Up to 670						
	P	AM4)	80% Calibrated	Up to	365		
Output Amplitude	High R	ate (NRZ &	Advanced Mode	Up to	mV		
	P	AM4)	80% Calibrated	Up to			
Patterns	Patterns			PRBS 7/9/11/13/15/23/31/58/9_4 SQ16, SQ32, LIN, CJT, SSPRQ, User Defined			
Transition time (20%	6-80%)	Low Rate		~14		20	
Transition time (20-8	80%)	High Rate		~12		ps	
littor		Low Rate		TBD		nc	
JILLEI		High Rate		TBD		hs	
Emphasis Resolutior				± 1000		Steps	

Table 2: TX output specifications



8. Receiver side characteristics

The receiver side characteristics are described in this section.

The BERT locks on different patterns, with the polarity inversion option. Real-Time BER can be measured. Histograms and SNR shared across all four channels. Independent CDR in each lane, being able to recover the supported rates.

Parameter		Typical Maximum	Unit
Line Rate	NRZ	22.75 – 29.25up to 29.25 (low rate45.5 – 56up to 56 (high rate)	e) Gbps
	PAM4	22.75 – 29.25up to 29.25 (low rate45.5 – 55.5up to 55.5 (high rate	e) Gbaud
Sensitivity	Low Rate	90	mV
Sensitivity	High Rate	100	
Patterns		PRBS 7/9/11/13/15/23/31	
CTLE		Adaptive (not manually controlled)	Steps

Table 3: Receiver specifications



9. ML4039EN characteristics

The ML4039EN has the same features as the ML4039E but in addition to that it also has a noise injection feature where the user can set and control the noise rate, pattern and amplitude being injected channel by channel.

Clock Configuration		Cor
Internal	Noise Injection	
Rate 25.7812! - GBaud	🔽 Enable N	loise
Apply Re	Rate	10.00919 -
BER BER Analysis		10.009191176470587
🔵 Moving Window BER 🥥	TX Mode	25.022977941176467
		25.7812499999999996 20.018382352941174
Relock		24.264705882352938
Continuous	Press Apply	for changes to take effects
O BER 10 -10		Mode Settings
Figure 5 : Noise injection	supported r	ates

10.Current revisions

The current revision of the ML4039E hardware is: ML4039E Rev C

All the listed features are tested using the following software and firmware:

- Software revision: MLBert_v.4.4.0.0
- Firmware revision:
 - ML4039E: ML4039E-Hyb_revC_FW_V3_0
 - o ML4039EN: ML4039EN_V1_0

11. Future Features

The following features will be implemented in the future ML4039E versions:

- FEC implementation
- External clock option



12.User Manual

12.1 GUI General Description

This section describes how to operate the ML4039E and all the capabilities of this BERT. The product software is available on the company's website on the below link: <u>https://multilaneinc.com/berts-gui/</u>

12.2 Installation

This chapter covers the installation of the instrument, addressing the following topics:

- System Start-up
- How to connect to the instrument

Note: For windows vista, 7, 8 and 10 users should always run the GUI as administrator.

First Steps

When the customer receives the instrument, it has a pre-configured IP address from the factory. This IP address is printed on a label on the instrument's back plate. The user can choose to keep this IP or to change it. If changing the IP is needed, there are two ways to do it: either through the USB interface, or through the Ethernet interface. If changing through USB is selected, then the USB driver of this instrument should be installed from the company's website, and the user needs to choose the application ETH config.

If the LAN interface is used to change the IP, then the user has to download the application "IPChanger" from the company's website and temporarily change his PC's IP to be in the same domain as the instrument, i.e. 172.16.xx.xx. Once the instrument's IP is successfully changed, the user can change back his PC's IP.

 It would be good if the user prints a label with the newly assigned IP address and sticks it on the instrument. If for some reason the IP is lost, the user will need to use the USB interface together with the ETHconfig software to "read" the IP.

Connect through Ethernet:

In order to connect via Ethernet, the IP address of the board is required. While no drivers are required; the user should simply know the current board IP address, and need to enter it in the text box next to the **IP** label, then click on the **connect** button.

The user can make sure that he is connected, by pinging the device.

To change the IP address of the board, the user needs to install the USB drivers. (Refer to paragraph 11.3).

After installing the setup, the user will be able to open the ML4039EGUI.



MLBert-GUI v.4.4.0.0 [MLBert API v4.1.1.0]									5 	ð ×	:
Help Internal Loopback (Disabled) Setup	SaveLoad Calibration	Enable CTLE									
multiLane						TX I RX I	OCK CHO	CH1 CH2 C	H3 CH4 CH5		°C °C
	Pattern Configuration										
IP 172.16.108.52 Connect	Label		TX Pattern	RX Pattern	Amplitude Range Amplitud	e Mid Eve Control	Pre-Emph	Post-Emp			
Clock Configuration	Cor	Ch 0									
Internal O External O Clk Out CDR		Ch 1		•	• •	•	•	*			
Rate 10 Gbps Rate /8 Clk Out		Ch 2	•	•	• •		•				
		Ch 3	•	•	• •	•	•	•			
Apply Ref 0 MHz		Ch 4	•	•	• •	-	•				
BER BER Analysis Vertical Bathtub JTOL		Ch 5	•	•	• •	•	•	•			
		Ch 6	•	•	• •	•	•	•			
O Instant BER O Real Time BER		Cn 7	•	•	• •	•	•	•			
Count (25 Kb) 10 🜩					Configuration						×
Multi Acquisition					BER						
Continuous		Ch1 - Ch2 - Ch3 - Ch3	Ch4 Ch5	Ch6 Ch7	1						
○ BER 10 -10 ◆	10'										1
		1									
	H 10 ⁰	1									
	E IV	1				÷			3		
									1		
V CHU V CHI V CH2 V CH3 V CH4 V CH5 V CH6 V CH7 Start	10 ⁻¹										
V CHO V CHI V CHI V CHI V CHI V CHI V CHI V CHI V CHI	10 ⁻¹ 0.0	0.2		0.4	0.6	0,	3	8	1.0	1	.2
V CHU V CHI V CHI V CHI V CH4 V CH5 V CH6 V CH7 Start	10 ⁻¹ 0.0	0.2		0.4	0.6 Acquisition	0.	3	8	1.0	1	.2
V CHU V CHI V CHI V CHI V CH4 V CH5 V CH6 V CH7 Start	10 ⁻¹ 0.0	0.2 Graph 🔘 Bathtub Cu	rve 🔘 Eye Cor	0.4	0.6 Acquisition athtub) Jitter Tolerance	0.1	3	Lay	1.0 out Type :) S	1 ingle () Mul	.2 ti
V CHU V CHI V CHI V CHI V CH4 V CH5 V CH6 V CH7 Start	10 ⁻¹ 0.0 Graph Type : BER	0.2 Graph () Bathtub Cu	rve 🔵 Eye Cor	0.4 ntour 🔿 V Ba	0.6 Acquisition	0.1	3	Lay	1.0 out Type : () S	1 ingle () Mul	.2 ti
V CHU V CHI V CHI V CHI V CH4 V CH5 CH6 V CH7 Start	10 ⁻¹ 0.0 Graph Type : O BER	0.2 Graph 🔘 Bathtub Cu	rve 🔵 Eye Cor	0.4 ntour 🔿 V Ba	0.6 Acquisition	0,1	3	Lay	out Type :) S	1 ingle () Mul	.2 ti
V CHU V CHI V CHI V CHI V CHI V CHI V CHI Start	10 ⁻¹ 0.0	0.2 Graph 🔘 Bathtub Cu	rve 🔿 Eye Cor	0.4	0.6 Acquisition athtub 🔿 Jitter Tolerance	0.1	3	Lay	000 Type : S	1 ingle 🔵 Mul	.2 ti

Figure 6: ML4039E GUI at start

12.3 Connecting Procedure

The user needs to connect using the board's IP, after that the board has been powered-up.



After clicking on Connect, all the Low voltage settings that have been saved during the calibration process are being applied. Also, the last used configuration is being applied.

Then the user can check the board's settings including the hardware ID and the firmware revision.

FWRev: 3 BoardID: 4244

Figure 8: ML4039E Firmware revision and Board ID

The displayed information is updated whenever any of the fields is being updated.



12.4 BERT Tab

At the first glance, after connecting to the board, the user will be able to detect on the GUI the: IP, Serial number, monitoring temperature, channels TX and RX lock, selected bit rate and all the clock configurations...

m MLBert-GUI v.4.4.0.0 [MLBert API v4.1.1.0]														800	٥	×
Help SaveLoad View												FV	VRev:3	1	BoardID :	4244
multiLane	« Confirmation											TX LOC RX LOC	CH1 CK	CH2	CH3 CH4	47°C 39°C
IP 172.16.108.52 Disconnect 🔹	Solution															
Clock Configuration	Sontr	TX Pa	attern Ar	nplitude					Error Ins	RX Pattern	DFE	1				
Internal External		Ch 1 User	defir *	391 -					Disabled •	PRBS 7 -	SLC -					
Rate 27.9524 - GBaud		Ch 2 User	defir 🕈	354 •					Disabled •	PRBS 9 -	SLC +					
Mode Settings -		Ch 3 User	defir 🔹	379 -					Disabled •	PRBS 7 -	SLC •					
Apply Ref 218.378125 MHz		Ch 4 User	defir ₹	369 -					Disabled *	PRBS 9 *	SLC -					
DED DED Analysis		Ch All	•						Disabled •	•	•	4				
Moving Window BER Real Time BER Relock							Configur	ation								
Continuous			~	OH 1			configur	ation	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		012				~	~
○ BER 10 -10 €	10 ¹							ю ¹								
O bits Count (Gb) 10 €	10 ⁻					-										
		100	8	Acquisition	1000	2			120	8	Acquise	ten	(557)		82	
V CH1 V CH2 V CH3 V CH4		2.4		04	0.5	12					04				1.4	
	Graph Type :	ER Graph	History	am O Ch	IR (dB)						Acquiel	1.50	out Type	.00	ingle (Multi
	ordbit iffer 1	er Graph C) Histogi	ani () si	(UD)				1			Lay	out type	• () 31	ingle 🥑	multi
Save Results																
Connected																

Figure 9: Main features detected after connecting

The user can select and control all the BERT settings.

Clock Configuration	S
Internal External Rate 27.9524 GBaud	Mode Settings -
Apply	Gray Mapping
BER BER Analysis	
🔘 Moving Window BER 🥥	
	TX Mode PAM4 -
Relock	Clock Out Monitor • 128 •
Continuous	
O BER 10 -1	Optimal Settings
O Bits Count (Gb)	Press Apply for changes to take effects
CH1 CH2	Mode Settings
Elevine 10. Data a	and also also and insuration of

Figure 10: Rate and clock configurations

The ML4039E supports in low and high rates both eye modes: NRZ and PAM4.



	Mode Settings +
Re	Gray Mapping 👿
<u> </u>	TX Mode PAM4 Clock Out PAM4 NRZ 128
-1	Optimal Settings
d (Press Apply for changes to take effects Mode Settings
	Figure 11: Supported eye modes

To switch between NRZ and PAM4 coding, use the TX Mode setting, then click Apply. The option Gray Mapping is only available in PAM4 mode. Gray Mapping enables use of PRBSxxQ defined in IEEE802.3bs. When Gray mapping is enabled, the PRBS13 and PRBS31 under the pattern select menu turn into PRBS13Q and PRBS31Q respectively.

For the clock configuration first select internal as the option (external clock-in option will be added in future ML4039E versions). The user now can select from mode settings between reference clock and monitor clock. For optimal results the Ref Clk should be selected.



Figure 12: Internal Clock Selection

For the monitor clock the output can be controlled based on the selected clock divider.



Mode Settings	•			
Gray Mappi	ng []		
TX Mode	PAM4	•		
Clock Out	Monitor	*	128 🔹	
			4	
			8	
	Optimal Se	ttings	16	
Pross Apply	for changes	to take	32	
FICSS ADDIV				
	Mode Settings Gray Mappi TX Mode Clock Out	Mode Settings - Gray Mapping TX Mode PAM4 Clock Out Monitor Optimal Se	Mode Settings • Gray Mapping	Mode Settings • Gray Mapping TX Mode PAM4 Clock Out Monitor 128 4 8 16 16

Figure 13: Monitor Clock-out options and dividers

For the line rate, the user can select any of the listed rates or enter any custom rate, but this rate should be in the supported range as described in table 2.

The user can control all the BERT configurations, channel by channel.

The test can be run in Low/High voltage settings mode or in advanced mode.



Figure 14: Selecting Advanced or Calibrated Settings mode

When operating in Low voltage settings mode, the Low voltage settings saved during the calibration process are being applied. And the user will be only able to control and change the amplitude. Based on the selected amplitude the software will automatically calculate the optimal settings.

Ch 1 User defit * 351 * Image: Character of the set of t		(Pattern /	Amplitude	 		Error Ins	RX Pattern	DFE
Ch 3 User defir * 379 * Image: Chai with the state w	Ch 2 Use	er defir *	354 •	 		 Disabled *	PRBS 7 *	SLC +
Ch 4 User defir * 369 * Disabled * PRES 9 * SLC * Ch All • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • <td>Ch 3 Use</td> <td>er defir 🔹</td> <td>379 •</td> <td></td> <td></td> <td>Disabled •</td> <td>PRBS 7 *</td> <td>SLC -</td>	Ch 3 Use	er defir 🔹	379 •			Disabled •	PRBS 7 *	SLC -
Ch All • Disabled • • • Auto-Relock	Ch 4 Use	er defir 🔻	369 •			Disabled •	PRBS 9 *	SLC •
Auto-Relock	Ch All	-				Disabled •	-	•
	Auto-R	Relock						

Figure 15: BERT side in Low Voltage settings mode

The ML4039E can output a wide range of pre-defined patterns. In addition to the PRBS patterns, there are linearity and jitter test patterns. Also, on top of the pre-defined patterns the user has the possibility of defining his own pattern.

Note: error detection only works on the PRBS patterns existing in the RX pattern drop down list. It is not possible to do error detection on custom defined patterns.





Figure 16: Pattern selection

In NRZ mode, for each level the corresponding eye amplitude is detected on the scope.



Figure 17: Amplitude control in NRZ mode and with the Low Voltage settings applied

In PAM4 mode, for each level the corresponding total eye amplitude is detected on the scope, this value is equal to the sum of the inner eye amplitude and two outer eye amplitudes. As shown in figure 17.



Figure 18: Amplitude control in PAM4 mode and with the Low Voltage settings applied

If the customer desires to control all the parameters, then he needs to go the advanced mode. While switching between advanced settings and calibrated settings modes the user will be modified that the optimal settings are being applied.



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Figure 19: Settings being applied

If advanced settings mode is selected, after clicking "OK" on the pop-up window shown in figure 18, the BERT configuration window will be displayed as follows and the user will have access to control the amplitude and the FFE taps:

	TX Pattern	Amplitude	Pre Emp	MainTap	Post Emp	InnerAmp	OuterAmp	Error Ins	RX Pattern	DFE
Ch 1	User defir 🔹	80 -	-58 *	912 -	-95 •	1000 -	2000 -	Disabled •	PRBS 7 *	SLC -
Ch 2	User defir 🔻	80 -	-58 *	849 -	-91 -	1000 -	2000 -	Disabled •	PRBS 9 *	SLC -
Ch 3	User defir 🔻	80 -	-58 *	486 -	-92 •	1000 -	2000 -	Disabled •	PRBS 7 *	SLC -
Ch 4	User defir 🔻	80 -	-59 *	838 -	-94 -	1000 -	2000 -	Disabled •	PRBS 9 *	SLC -
Ch All	•	-	•	-	•	•	-	Disabled •	•	•
🔳 Au	to-Relock									

Figure 20: BERT Configurations in PAM4 and Advanced Mode with 3 taps option

Main-Tap, Pre and Post Emphasis level varies between ± 1000 . The amplitude slider does not show anymore the values that have been saved during the calibration. The user can go up to 120% and the corresponding amplitude is detected on a scope.

To access the 7 taps FIR the user should select the advanced settings then go to the mode settings tab and enable the 7 taps option, and press apply.





The user can test the BER, histogram and SNR, on the selected channels.

Error insertion can be controlled channel by channel.

All these measurements can be performed on all the rates, patterns and in NRZ and PAM4 modes. Below are shown some screenshots showing the eye in PAM4 and NRZ modes. These screenshots are captured, with the 80% calibrated settings being applied.



Figure 23: PAM4 mode, low rate



Figure 24: NRZ mode, low rate



Figure 25: NRZ mode, high rate





Figure 26: PAM4 mode, High rate with PTB

Figure 26 shows the 7 taps settings that are used to capture figure 27(NRZ eye) and 28 (PAM4 eye).





Figure 28: Captured eye in NRZ mode using 7 taps settings





Figure 29: Captured eye in PAM4 mode using 7 taps settings

12.5 BERT measurements

To be able to start BER measurements, the instrument ports should be in loopback mode, which means the TX ports should be connected to the RX ports and the PPG and ED patterns should match. It is not necessarily to supply a PRBS from the same physical instrument – the source can be a different instrument and the error-detector of the ML4039E can derive its own clock from the received data (no need for a separate clock link). However, if Gray coding is used in the source, one should tell the receiver to expect Gray coding as well. There should be a match in pattern, polarity and coding to have lock.

The user can run the BER test on selected channels continuously or choose a target BER or set a timer.

BER	BER Analysis
	🔿 Moving Window BER 🥥 Real Time BER
-	
	Relock
(Ontinuous
(⊖ BER 10 -10 🕏
(Bits Count (Gb)
(Timer 00 d 00 h 00 m 30 s
	🕅 CH1 🕼 CH2 🕼 CH3 🕼 CH4
	Start

Figure 30: BER control panel

The BER values are displayed per channel and their corresponding BER graph. In PAM4 the value of the BER at MSB and LSB is shown. The graph shows the total BER value.



	t 🔹	Ch2 Bit Error Count BER Bit Error Count MSB BER MSB Bit Error Count LSB BER LSB	0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00	
ts			Save Results	
lues in	RZ mode	Figure 32: B	ER values in PAM	l4 mode



Figure 33: BER test on 4 channels

The user can test the BER, histogram and SNR, on the selected channel, in NRZ and PAM4 modes.

BEK	BEF	(Analysi	S			
<u></u>	listo	gram		\bigcirc	Signal to	Noise Ratio
			Clea	r All		
Ch 1	Sta	rt Ch	2 Start	Ch 3	Start	Ch 4 Start
		Figu	re 34: BE	R analy	sis tab	



班 MLBert-GUI v.4.4.0.0 [MLBert API v4.1.1.0]												– ć	5 X
Help SaveLoad View										FWRe	v:3	Boa	rdID : 4244
multiLane										TX LOCK RX LOCK	CH1	CH2 CH3	CH4 54%
IP 172.16.108.52 Disconnect 🔹	《 Configuration												
Clock Configuration	Cont	TX Pattern	Amplitude			Err	or Ins F	RX Pattern	DFE	1			
Internal External	Ch 1	PRBS 7 *	207 -			Disa	bled •	PRBS 7 •	SLC -				
Rate 52 125 - GRand	Ch 2	PRBS 7 *	193 •			Disa	bled •	PRBS 7 *	SLC *				
Mode Settings -	Ch 3	PRBS 7 *	204 -			Disa	bled •	PRBS 7 *	SLC •				
Apply Ref 156.25 MHz	Ch 4	PRBS 7 *	199 -			Disa	bled •	PRBS 7 *	SLC -				
	Ch All	•				Disa	bled •	•	•				
Clear All Ch 1 Start Ch 2 Start Ch 3 Start Ch 4 Start					Configu	ration				Å		Å	8
Bit Count 2.729e+13	4 4 4	4 *	in .				4					3	- × - ×
BER Error Count Ch1 0.00e+00 0.00e+00 Ch2 0.00e+00 0.00e+00 Ch3 0.00e+00 0.00e+00 Ch4 0.00e+00 0.00e+00		ļ								4	-	Å	
	Graph Type : 🔘 BER Gra	ph 🍥 Histo	ogram 🔿 SNR	dB)			I			Layout	Туре	: Single	e 🧼 Multi
Save Results													





Figure 36: SNR in PAM4 mode

This BERT gives the user the possibility to insert errors by enabling the error insertion option.

Ins RX Pattern	DFE	
led • PRBS 7 •	SLC -	
👿 Enable Word Gap	1 (8 bits	; block) Continuous
Mode	128 Errors per fra	rame 🔹
	128 Errors per	frame
	Error Insertion	







Hei Section Vew PWRe: 3 Bandlib::240 H MULTI and # CHI CRO CRI CRO CRI	📅 MLBert-GUI v.4.4.0.0 [MLBert API v4.1.1.0]										-	٥	×
Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Control Contro <td< th=""><th>Help SaveLoad View</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>FWRev :</th><th>3</th><th>BoardID</th><th>: 4244</th></td<>	Help SaveLoad View									FWRev :	3	BoardID	: 4244
IP T22.16.108.52 Disconnect Configuration IP T22.16.108.52 Disconnect IP	multiLane									TX LOCK	11 CH2	СНЗ СН	4 53*C 45*C
Cock Configuration Error Im. Ko Kattern OPE Rate	IP 172.16.108.52 Disconnect	Configuration											_
Merral Extended Fills	Clock Configuration	Cont	TX Pattern	Amplitude			Error Ins	RX Pattern	DFE				
Ref 26.023 Past 7 103 - Enabled / First 7 SLC - Apply Ref 156.23 Mitz Ref SLC - SLC - BER Reform Ref 156.23 Mitz Image 7 103 - Image 7 SLC - SLC - BER BER Reform SLC - Image 7 SLC -	Internal External	Ch 1	PRBS 7 *	207 •			Enabled *	PRBS 7 *	SLC -				
Ref Ref There	Pata ac rear CRaud	Ch 2	PRBS 7 *	193 -			Enabled •	PRBS 7 *	SLC -				
Agely Bef 150-25 Mitz BER REF Analysis Conditionance Con	Mode Settings -	Ch 3	PRBS 7 *	204 -			Enabled •	PRBS 7 *	SLC •				
BRR BRANAYSIS BRR Moving Window BLR @ Real Time BLR Releack Continuous BRR 10 - 10 @ BIS Count (40) Timer 1075 Start Timer 1075 Symbolic Count 4.445+112 BR Couph Type : @ BER Graph Thistogram O SHR (48)	Apply Ref 156.25 MHz	Ch 4	PRBS 7 *	199 •			Enabled •	PRBS 7 *	SLC •				
BER Moving Window BER Relack Continuous 0 10 Bits Count (0k) 10 0 Timer 0 0 Start 0 0 Timer 107 0 Start 0 0 Bit Count 8.891e+12 0 Chil workey & 200x 00 00 0		Ch All	•				Enabled •						
Continuous DER 10 DER 10 Diss Count (ch) 10 Diss Count (ch) 0 0 0 0 0 Timer 1075 Symbol Count 8.891e+12 Chi month 8.891e+12 Chi	Moving Window BER Real Time BER Relock												
BER 10 10 10 Bits Count (20) 10 10 10 Timer 00 400 h 00 m 00 s b 10 10 If	Continuous			201		Configurat	ion		194				÷
Bits Count (6) 10 Bits Count (6) Timer 00 d 00 h 00 m 30 s (2) Start 10 Bits Count (4) Start 10 Bits Count (4) Signable Count (445e+12) Bits Count (445e+12) Bits Count (8,891e+12) Ch1 Ch1 200 m0	-10 DE	4.,		_			4.3						
Bits Count (6b) 0 d @ 0, 0 m 35 ± CH1 C H2 Start There 1975 Symbol Count 4.445e+12 Bits Count 8.891e+12 Ch1 Ch1 Ch1 Count 0 Start Start		5		_									
Timer 00 d00 h 00 m 0 3 2 Image: Image: Start Timer 107:s Symbol Count: 4.45e+12 Bit Count: 8.89fe+12 Chil Image: Chil Start Image: 0.00 m0 m0 3 2 Image: 0.00 m0 m	Bits Count (Gb)	39	1				10'0					1	
Image: Chi III Chi III Chi III Chi IIII Chi IIII Chi IIII Chi IIIIIIIIII	○ Timer 00 d 00 h 00 m 30 s 🚍	· · · ·	80 ET	Bi 100 Accuration UNP'R	117 154 1	r	е п	22 80	er si Activistion (1	9"R 10	<u>0</u>	54 (B)	
Start Timer 1975 Symbol Count 4.45s+12 Bit Count 8.891e+12 Chi count 9.580 mm Chi count 9.580 mm	CH1 CH2 CH3 CH4	***		04			**		014				_
Start Immer 167.5 Symbol Count: 4.445e+12 Excount: 8.89fe+12 Chil Chil Chil 2.00x, 00		K		A design of the local data in the local data	1				ton and so and	Concernance of the local division of the loc		1 1	
Timer 1975 Image: Symbol Count. 4.445e+12. Image: Symbol Count. Image: Symbo	Start					·						-	
Symbol Count 4.445e+12 Graph Type : BER Graph Histogram SNR (dB) Layout Type : Single Multi	Timer 167s	4.0	20 P				4.0	20 80	e 9	100 1		a a	
Bit Count 8.891e+12 Ch1 Information and a state of the	Symbol Count 4.445e+12	Coult Turne Courses		Algorithm (1772					Assessed	73	-		
	Bit Count 8.891e+12	Graph Type : O BER Gra	ph 🔘 Histo	ogram 🔿 SNR (di	5)		1			Layout ly	pe : ()	Single 🥥	Multi
	Ch1												
Save Results	Save Results												

Figure 39: BER measurement with 1 error inserted at the MSB and 1 error at the LSB

The user can choose among two DSP modes: slicer for non-strenuous links and slicer with reflection canceller.

	Error Ins	RX Pattern	DFE					
	Enabled •	PRBS 7 🔻	SLC -					
1	DSP mode	Slicer w	ith reflection can					
		Slicer f	or non strenuous					
		Slicer v	vith reflection can					
	Please click the "Set" button to apply changes.							
			Set					
			DFE Lev					
_		Figu	ure 40: DSP mo					

12.6 ML4039EN Noise injection

The same is applicable for the ML4039EN with an additional noise injection feature. When connected to an ML4039EN and additional noise injection tab will show in clock configuration.

IP	172.16.109.90		Disconnect
Clock Conf	iguration		
) Rate	Internal		Noise Injection •
	Apply	Re	Mode Settings • f 151.654411 MHz

Figure 41: noise injection tab

To access noise injection settings the user should first enable noise injection and pick a rate from the drop down list also choose the preferred TX mode: PAM4 or NRZ (note that PAM4 is not available at rate 10.009191176470587) and press apply.



	Noise Injection •	
Re	Rate 25.02297 -	Clock Configuration
0	TX Mode PAM4 •	Rate 25.7812! - Gbps Noise Injection -
	Apply	BER BER Analysis 10.009191176470587 Moving Window BER (a) TX Mode 25.022977941176467 25.78124999999996 25.78124999999996
	Press Apply for changes to take effects	Relock 20.0183823529411/4 Q4.264705882352938 Ochinuous Press Apply for changes to take effects
-11 Figur	Mode Settings re 42: noise rate and TX mode for noise	BER 10 Mode Settings Figure 43: available noise rates

After pressing apply a new noise row will appear on the configuration table for each channel where the user will be able to control the noise pattern and amplitude.

on											
								_			
_		TX Pattern	Amplitude	Pre Emp	MainTap	Post Emp	InnerAmp	OuterAmp	Error Ins	RX Pattern	DFE
C	Ch 1	PRBS 7 *	80 -	-157 •	1000 -	-109 -	1000 -	2000 -	Disabled •	PRBS 9 *	SLC •
N	loise1	PRBS 7 -	120 -		0 -						
C	Ch 2	PRBS 7 *	80 -	-100 -	1000 -	-93 •	1000 -	2000 -	Disabled •	PRBS 7 *	SLC -
N	loise2	PRBS 7 -	60 -		1000 -						
C	Ch 3	PRBS 7 *	80 -	-543 •	28 -	-529 •	1000 -	2000 -	Disabled •	PRBS 7 *	SLC -
N	loise3	PRBS 7 -	60 -		1000 -						
C	Ch 4	PRBS 7 *	80 -	-524 •	39 •	-538 •	1000 -	2000 -	Disabled •	PRBS 7 *	SLC -
N	loise4	PRBS 7 •	60 -		1000 -						
	Aut	o-Relock									
		ORCIOCK									

Figure 44: configuration table after enabling noise injection

Below are some screenshots showing the noise being injected at different rates to a 53.125 PAM4 signal.





Figure 46: noise being injected at rate 10.3125 and main tap 1000

Figure 45: PAM4 clean eye







Figure 48: noise being injected at rate 25.78125 and main tap 1000

13.IP changer tool

If the user needs to change the IP of the board, the link represented below, has all needed tools (software and user guide).

https://multilaneinc.com/berts-gui/







Setup MLIPChanger-v1.2

ML IP Changer Guide V 11

Figure 49: IP changer GUI and User Guide

Figure 50: Ethernet Configuration Software

ML4039-eth-configuration-



14. Revision History

Revision number	Date	Description
1.0	11/14/2019	 Document created
1.1	11/18/2019	 Added ML4039EN characteristics and user manual



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